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DESIGN AND IMPLEMENTATION OF IP CORE FOR ROADRUNNER-128 BLOCK CIPHER

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Overview

- ABSTRACT
- INTRODUCTION
- STRUCTURE AND DESIGN OF RRR-128
- FPGA IMPLEMENTATION
- RESULTS AND COMPARISONS
- CONCLUSION

Abstract

- **RoadRunneR-128 -** Recently invented light-weight block cipher, specifically designed for 8-bit platforms [1].

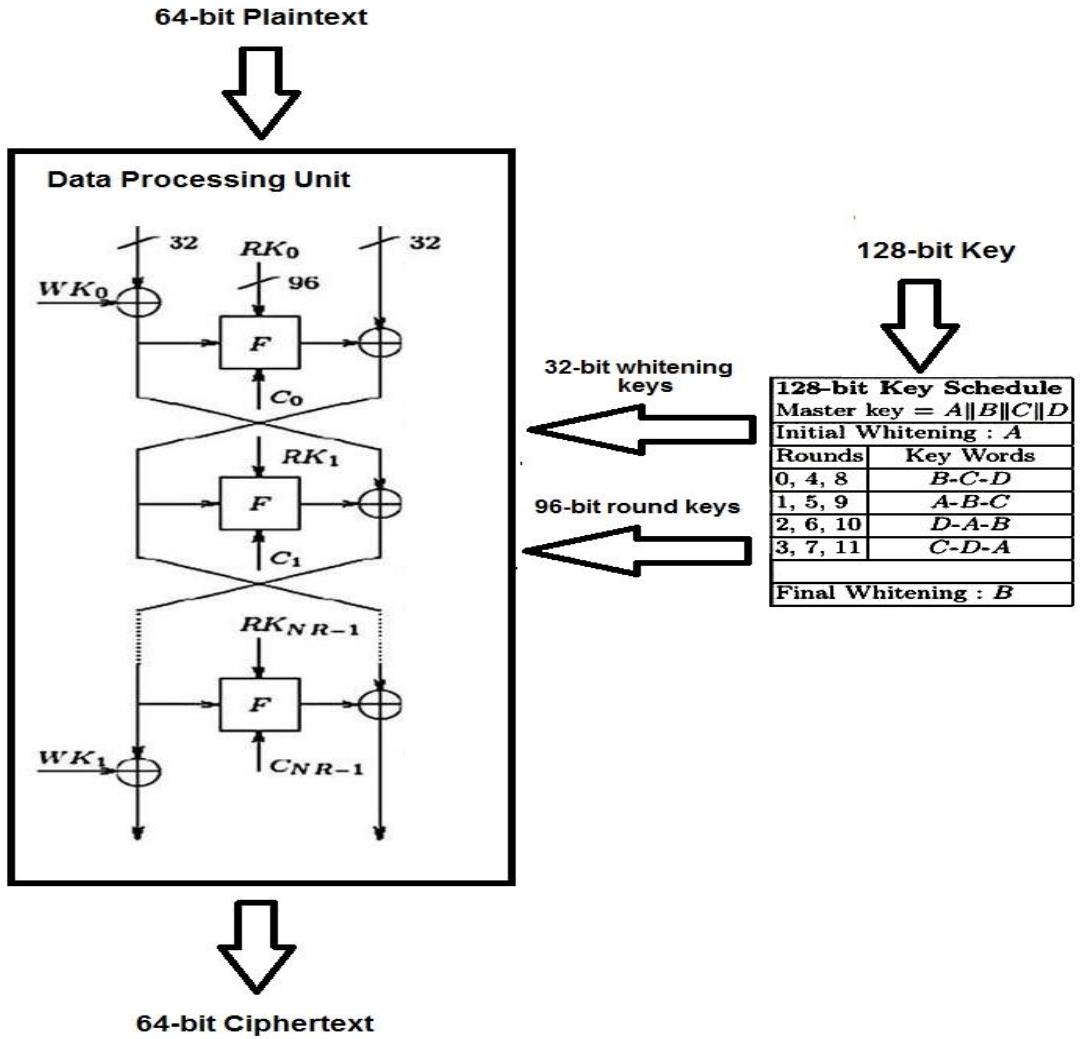
- Design and hardware implementation of IP core for RoadRunneR-128 on FPGA.

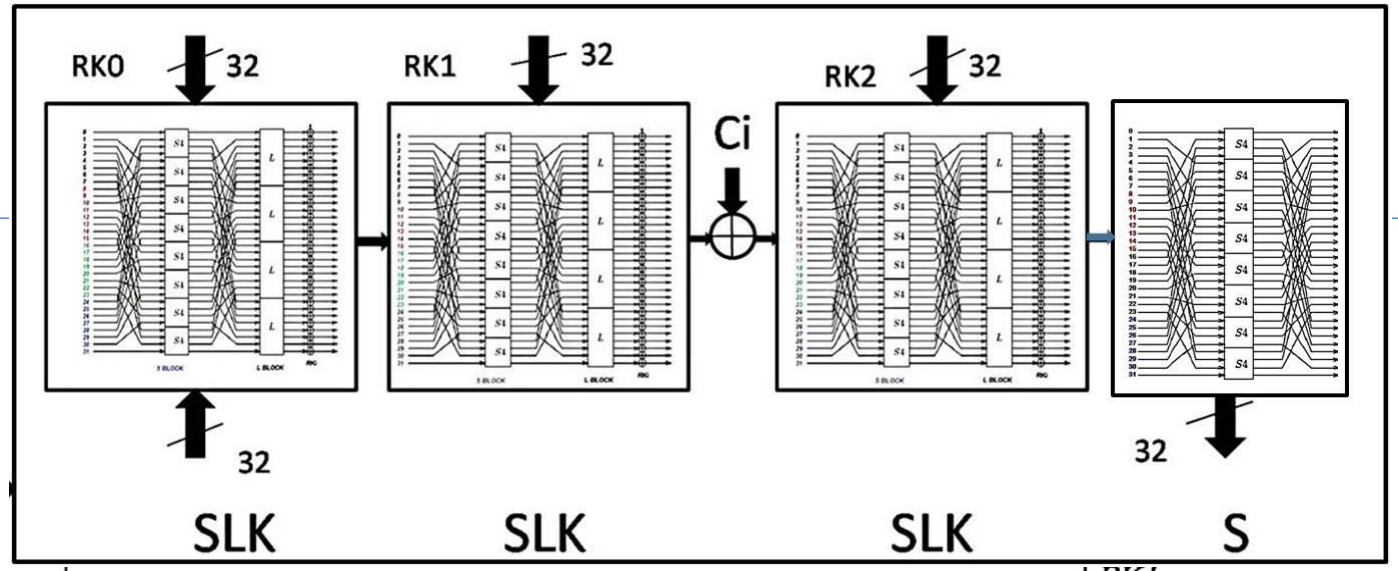
- Evaluation of performance , resource utilization and estimated power consumption of the design on FPGA.

Introduction

- **RoadRunneR-128** is a small and fast Bitslice Block cipher**.**
- Feistel structure**.**
- Key length - 128 bit, Block length - 64 bit.
- Highly optimised for software implementation on 8-bit CPUs.
- Proven security against different cryptographic attacks [1]**.**

Structure of RoadRunneR-128





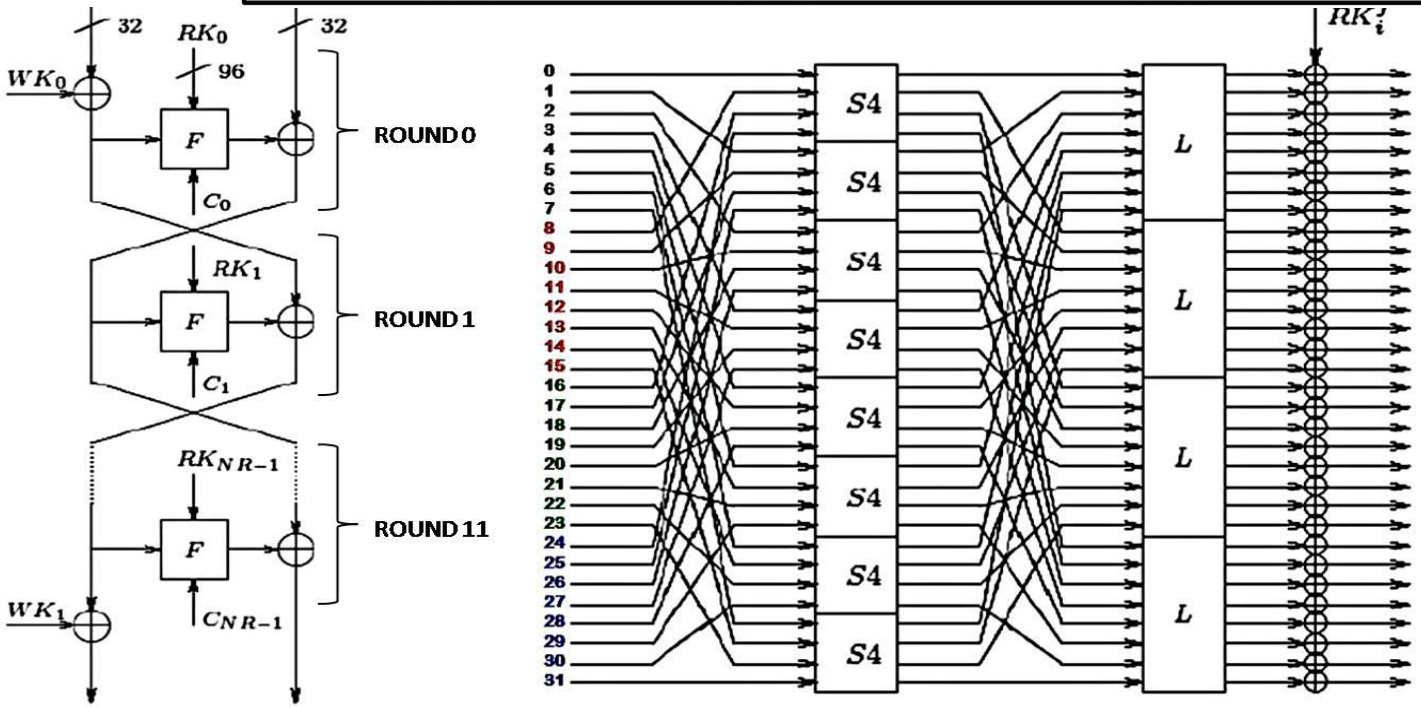
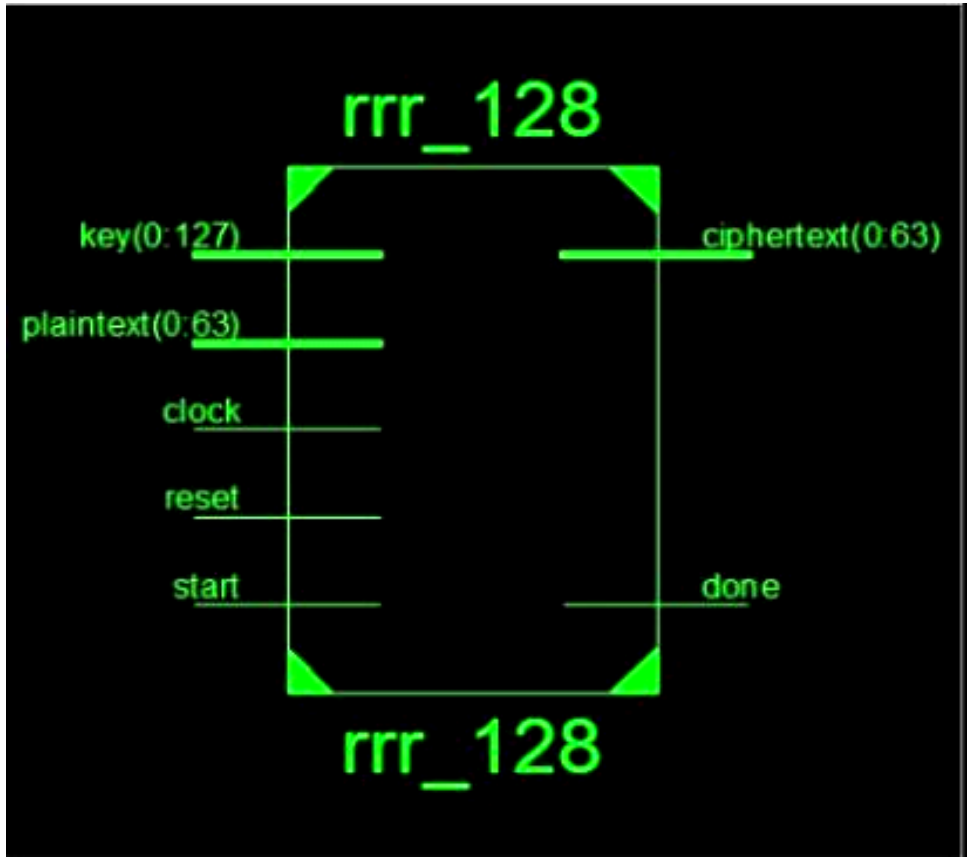


Fig.1 : Detailed diagram

RTL Design

- Data processing and key generation units.
- Designed using Verilog HDL – as finite state machine.
- Pipelining of complex logic to multiple clock cycles.
- 22 clock cycles per round.
- State encoding for low power.
- Test bench development and RTL simulation using Modelsim.

RRR-128 Core's Interface



FPGA Implementation

- Synthesized using Quartus II for Altera FPGA.
- Balanced optimization – Area and speed.
- Successfully verified the timing and analyzed the power.
- Tested in Altera DE1 Cyclone II FPGA.

Simulation and Implementation Results

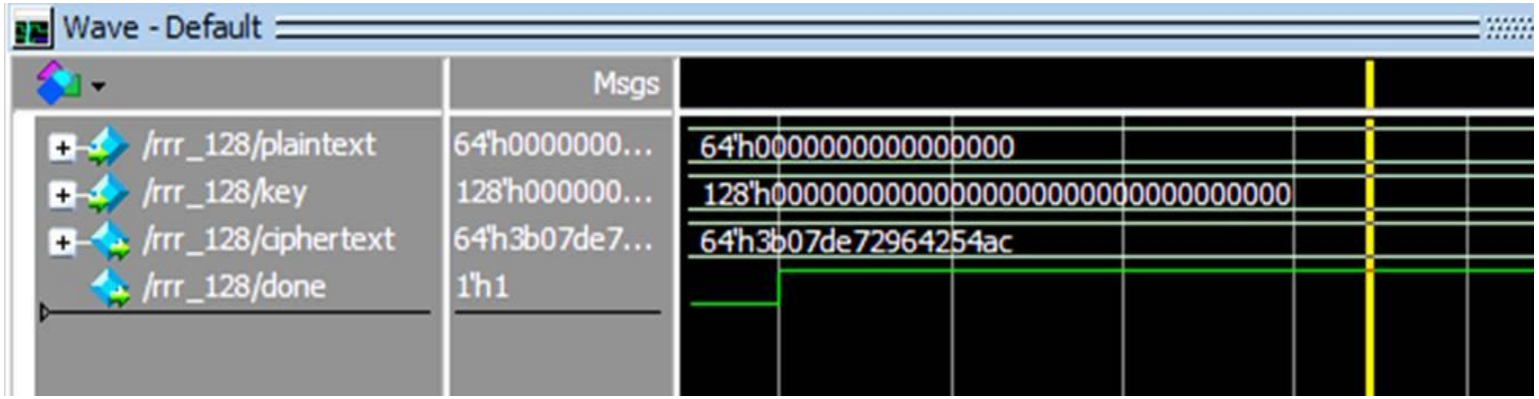


Fig. : RTL Simulation in ModelSim

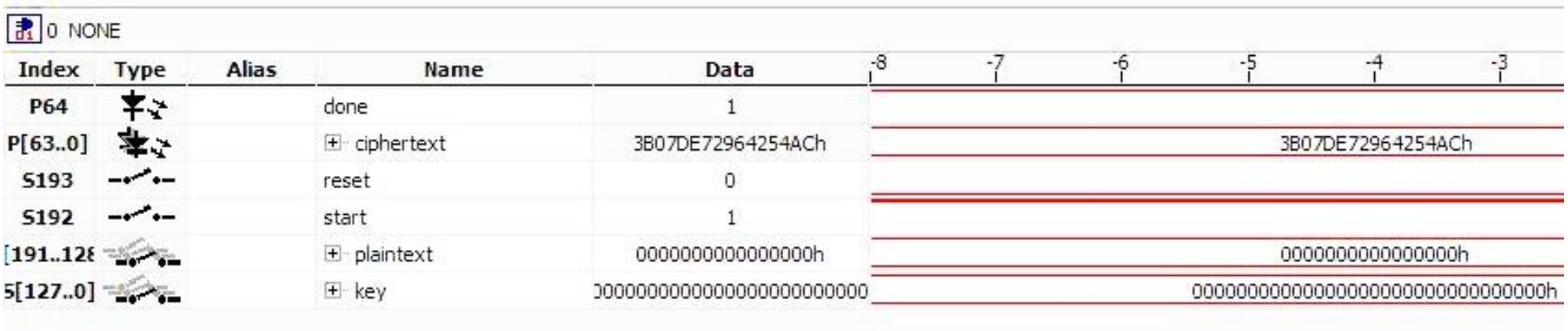


Fig. :Implementation Result in QUARTUS II In-System Memory Content Editor

Results

PERFORMANCE METRIC	
Total area	2% of the hardware (802/33216 Logic Elements)
Maximum clock frequency of operation	272.18 MHz
Estimated power consumption	140.74 mW
Clock cycles to perform the encryption	268 clock cycles
Total encryption time	0.98 µs
Throughput for the implementation	65 Mbps.
Throughput per Area Efficiency	0.081 Mbps/slice

Comparison with other ciphers

Cipher	FPGA/ASIC	Area Utilization	Throughput
RRR-128	Altera DE1 cyclone II FPGA	**2%**	65 Mbps
RRR-128 *[11]*	0.18µs CMOS - ASIC	1400 GE	156 Kbps
Triple DES *[13]*	Altera DE1 cyclone II FPGA	40%	3 Gbps
Curupira – 1 *[14]*	Altera DE1 cyclone II FPGA	40%	200 Kbps
AES-128 *[6]*	Altera DE1 cyclone II FPGA	56%	1.5 Gbps

Cipher	Attacked Rounds
RRR-128 [1]	**6/12**
AES	7/10
PRIDE	26/31
SPECK-128	17/27
PRESENT	26/31
SIMON	26/42

Test Vector Generation Tool

Fig. : RRR-128 Encryptor

Test Vectors

PLAIN TEXT	KEY	CIPHER TEXT
0000_0000_0000_0002	8000_0000_0000_0000 0000_0000_0000_0000	C168_C69A_C195_845E
0010_0020_0030_0040	0000_0000_0000_0001 0000_0000_0000_0001	3109_48CF_D78E_57B4
0010_0200_0000_0000	0001_0000_0000_0001 0001_0000_0000_0001	52BB_4E1A_331D_91BF
FEDC_3210_0002_0000	0123_4567_0000_CDEF 0123_4567_0000_CDEF	E45B_1D93_75E2_7364
1000_1002_5000_4000	1111_2222_3333_4444 1111_2222_3333_4444	0DF2_9A4F_C5BF_5BFF
1023_2050_1147_8124	1000_4000_5000_2222 1000_4000_5000_2222	BB76_8D15_1B18_616F

Conclusion

- Designed and implemented a soft IP core for RoadRunneR-128 block cipher on Altera DE1 cyclone II FPGA.
- Verified functionality and tested on-board.
- Lesser area utilization, reasonable throughput- light weight applications.
- Outperforms its previous implementation, by over 400 times in terms of throughput.
- The work is the first of its kind – further improvement in future.

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